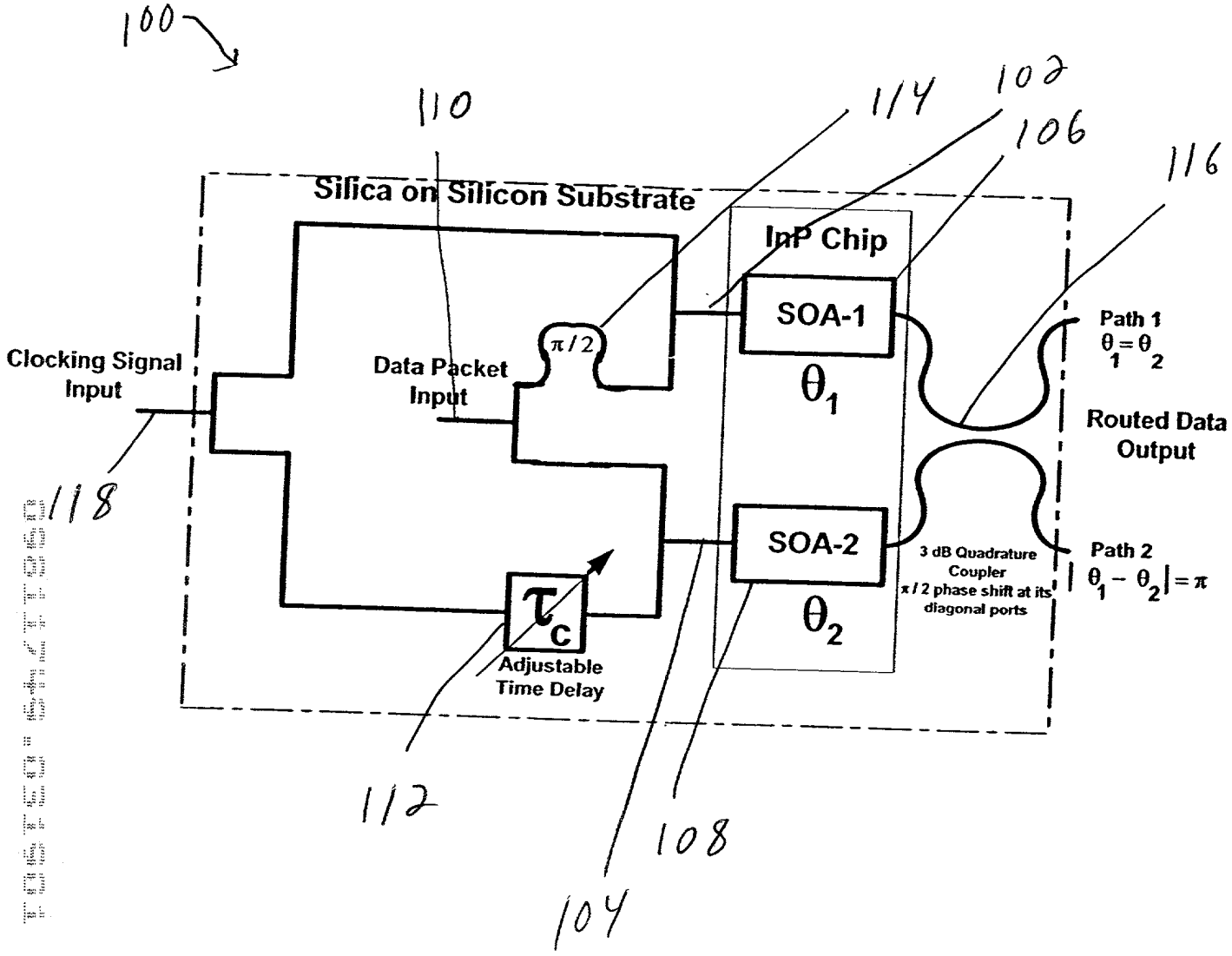
100
110
114
102
106
116
Silica on Silicon Substrate
InP Chip
SOA-1
θ_1
Path 1
$\theta_1 = \theta_2$
Routed Data
Output
Clocking Signal
Input
118
Data Packet
Input
$\pi/2$
SOA-2
θ_2
3 dB Quadrature
Coupler
$\pi/2$ phase shift at its
diagonal ports
Path 2
$|\theta_1 - \theta_2| = \pi$
τ_c
Adjustable
Time Delay
112
108
104

Fig. 1

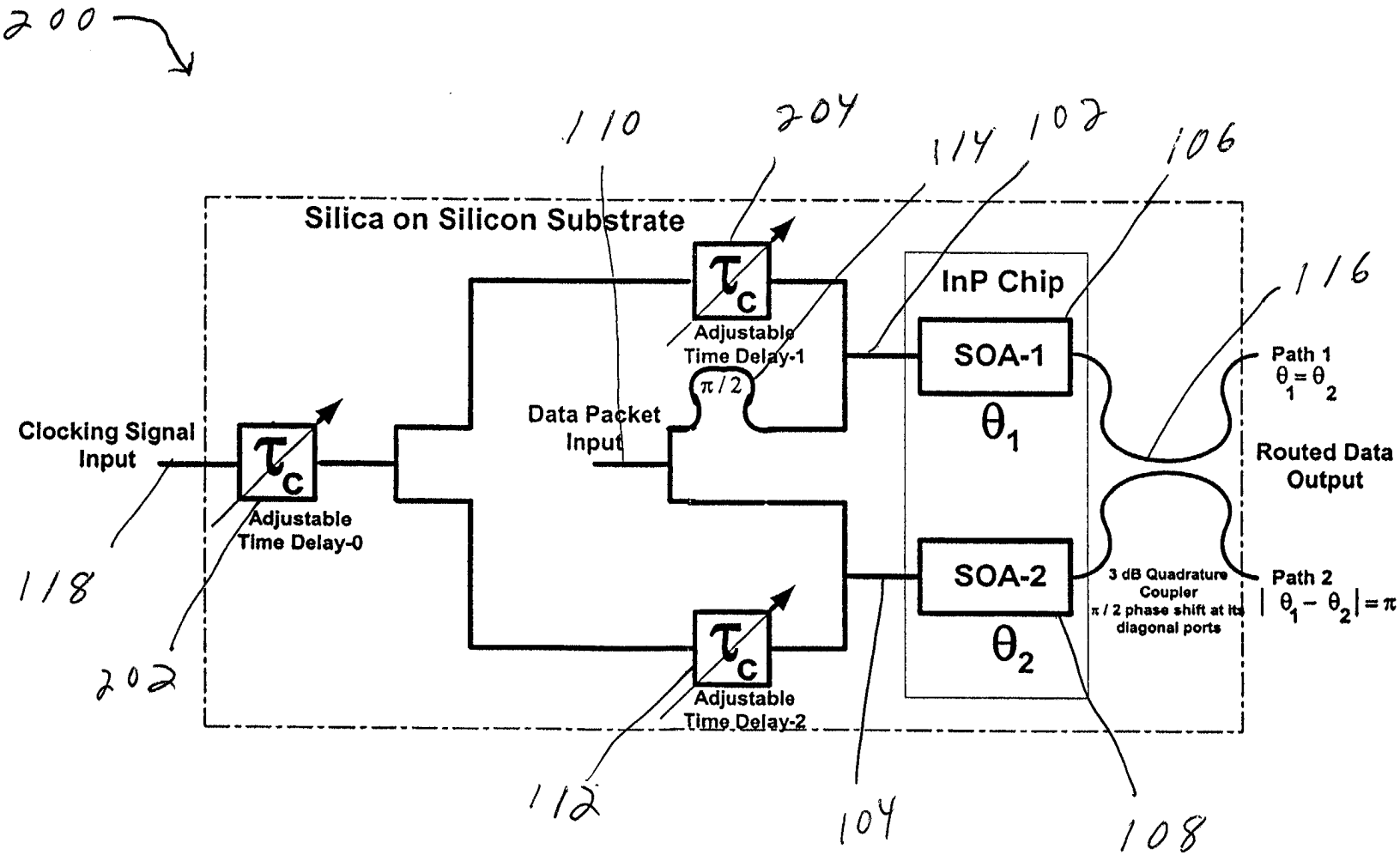

FIG. 2

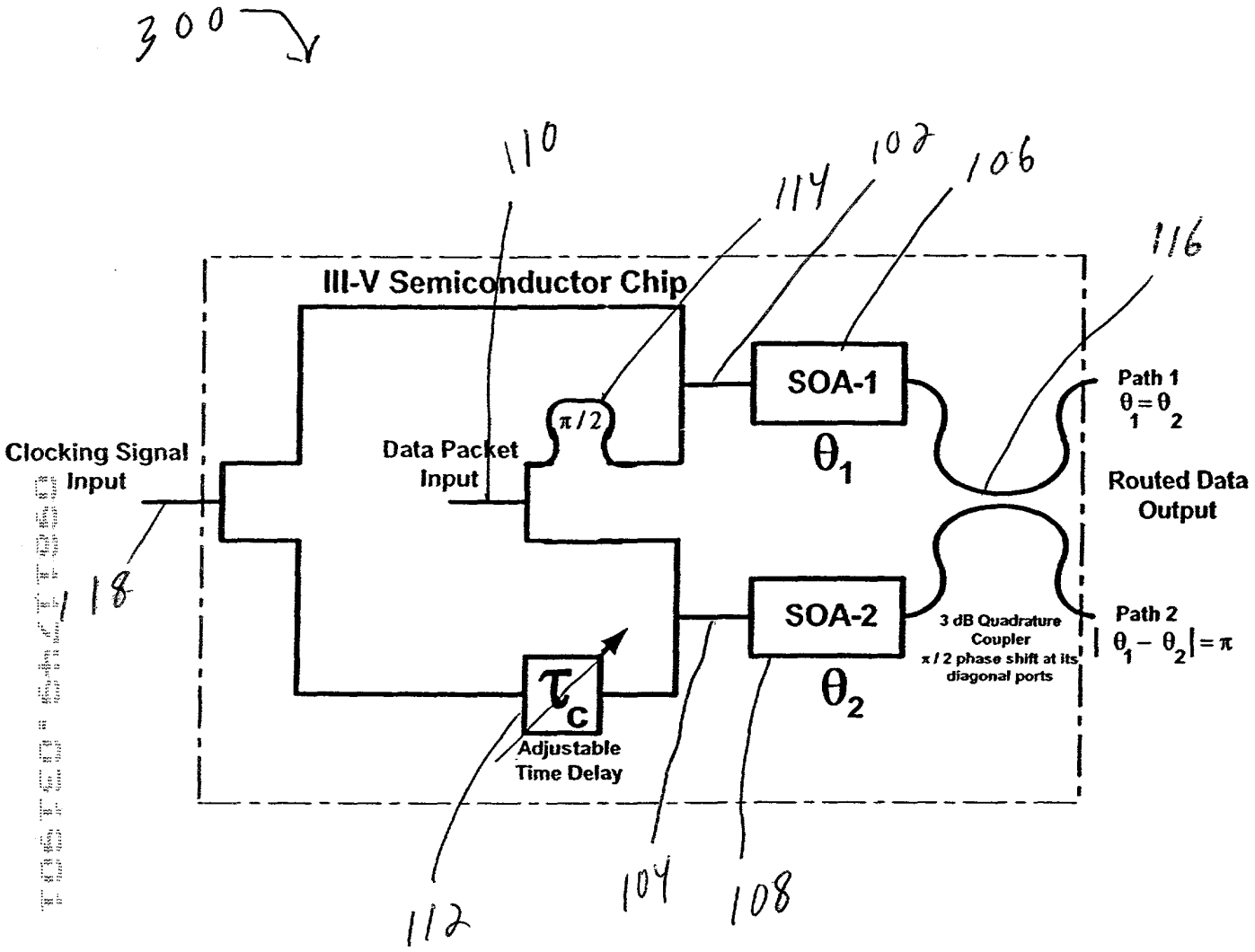
300
110
114
102
106
116
III-V Semiconductor Chip
Clocking Signal Input
18
Data Packet Input
π/2
SOA-1
θ1
Path 1
θ1 = θ2
Routed Data Output
SOA-2
θ2
3 dB Quadrature Coupler
π/2 phase shift at its diagonal ports
Path 2
|θ1 − θ2| = π
τc
Adjustable Time Delay
112
104
108

Fig. 3

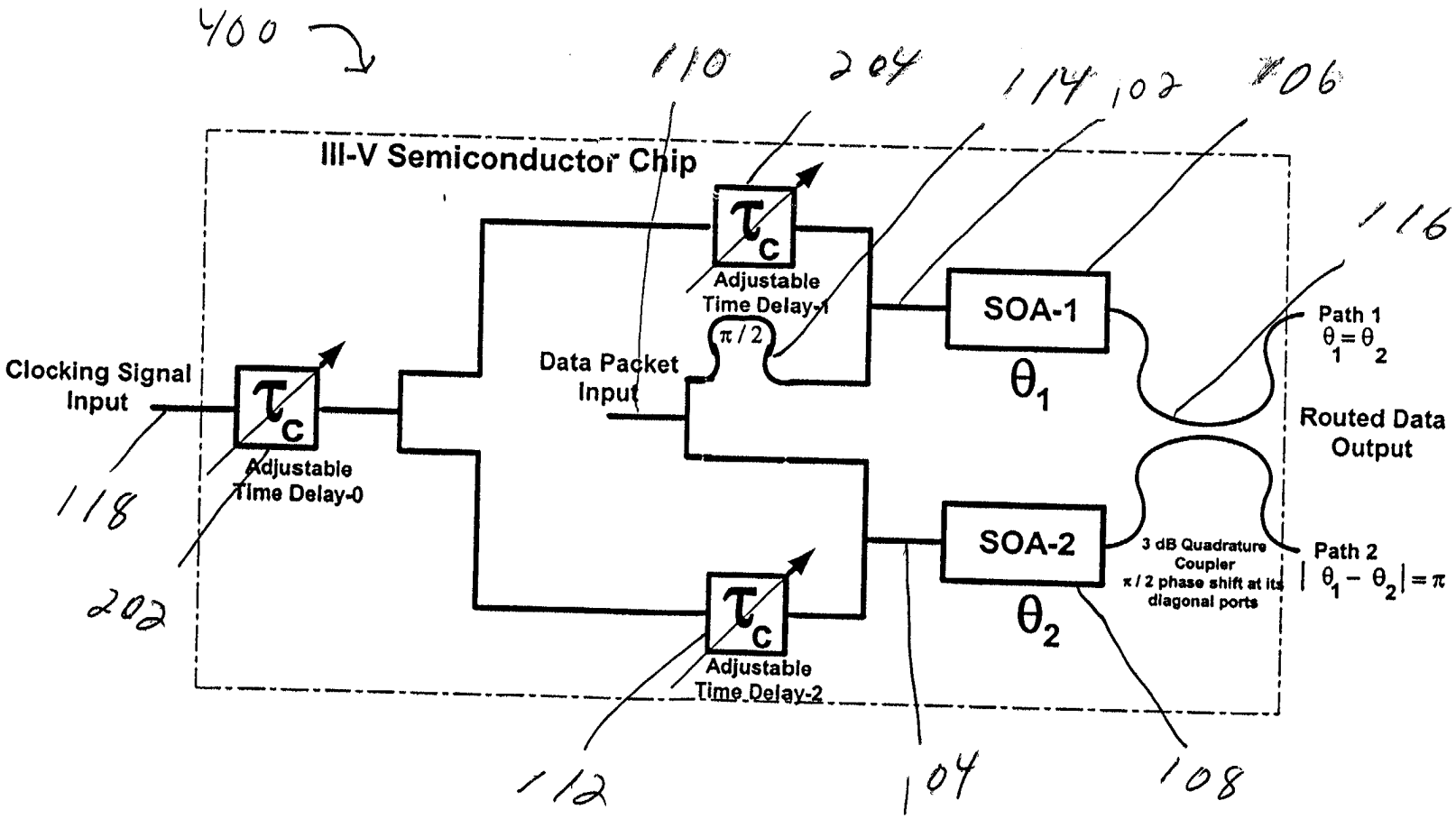
400
110
204
114
102
106
116
III-V Semiconductor Chip
Adjustable Time Delay-1
π / 2
SOA-1
θ1
Path 1
θ1 = θ2
Clocking Signal Input
Data Packet Input
Routed Data Output
118
Adjustable Time Delay-0
202
SOA-2
θ2
3 dB Quadrature Coupler
π / 2 phase shift at its diagonal ports
Path 2
|θ1 − θ2| = π
Adjustable Time Delay-2
112
104
108

FIG. 4

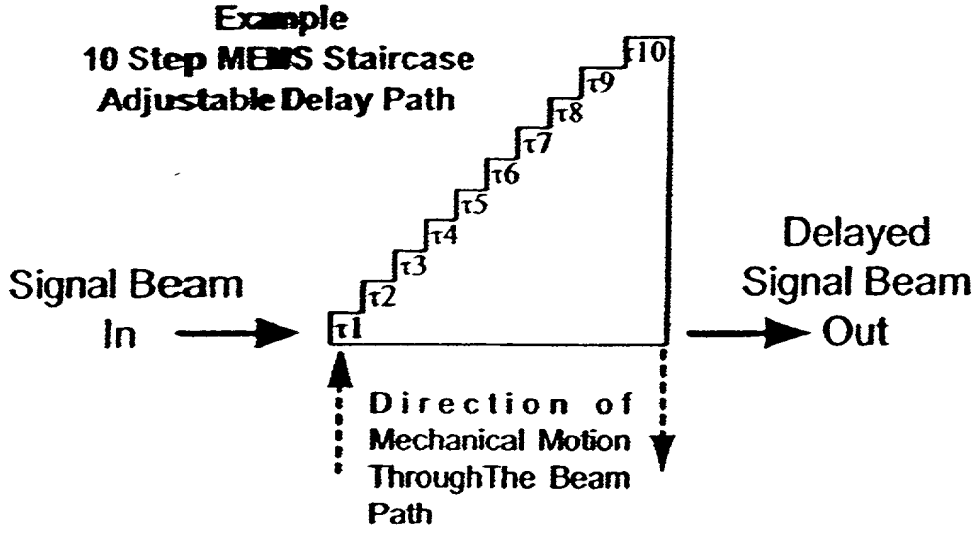
Example
10 Step MEMS Staircase
Adjustable Delay Path
τ1
τ2
τ3
τ4
τ5
τ6
τ7
τ8
τ9
τ10
Signal Beam
In
Delayed
Signal Beam
Out
Direction of
Mechanical Motion
Through The Beam
Path

Fig. 5

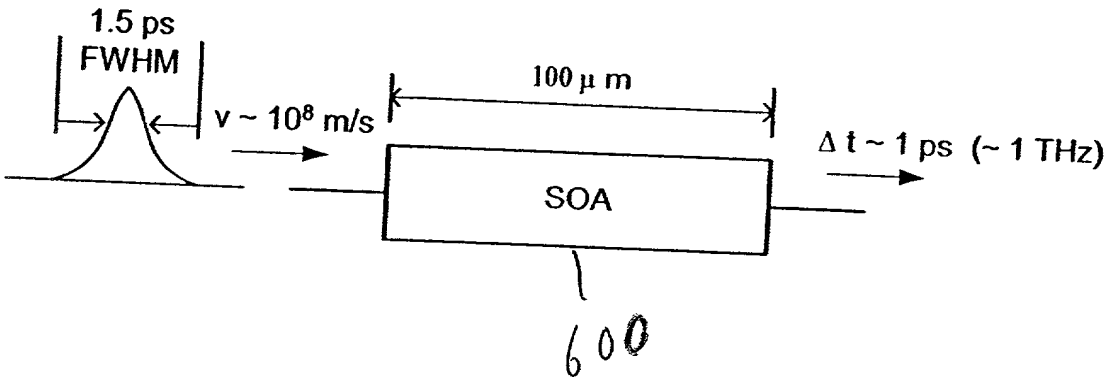

Fig. 6

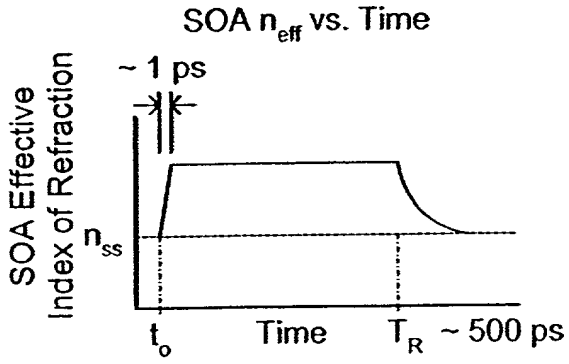
SOA n_{eff} vs. Time
~ 1 ps
SOA Effective
Index of Refraction
n_{ss}
t_o
Time
T_R ~ 500 ps

Fig. 7

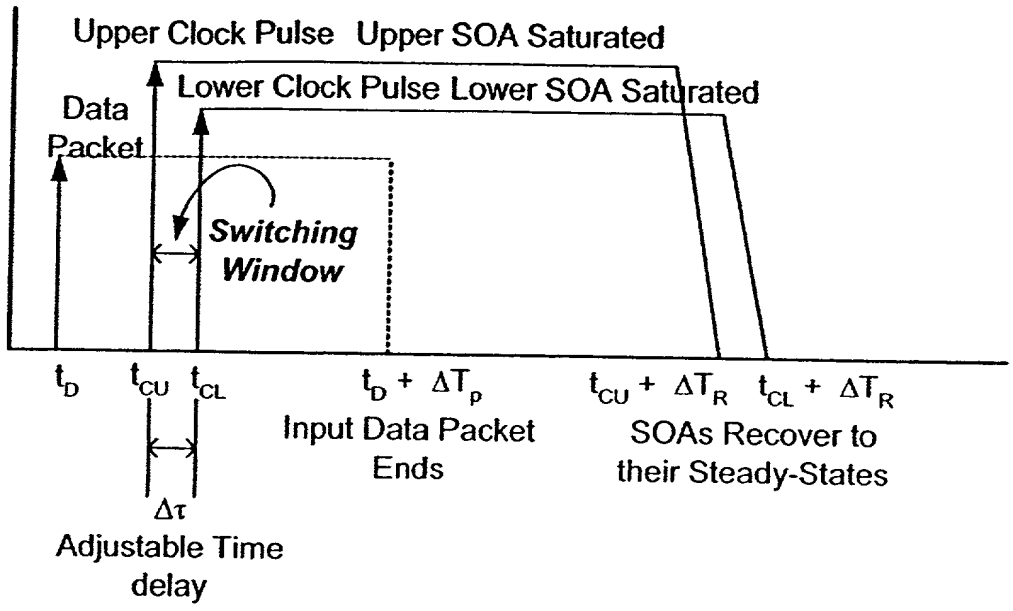
Upper Clock Pulse Upper SOA Saturated
Lower Clock Pulse Lower SOA Saturated
Data Packet
Switching Window
t_D
t_{CU}
t_{CL}
$t_D + \Delta T_p$
Input Data Packet Ends
$t_{CU} + \Delta T_R$
$t_{CL} + \Delta T_R$
SOAs Recover to their Steady-States
$\Delta\tau$
Adjustable Time delay

Fig. 8

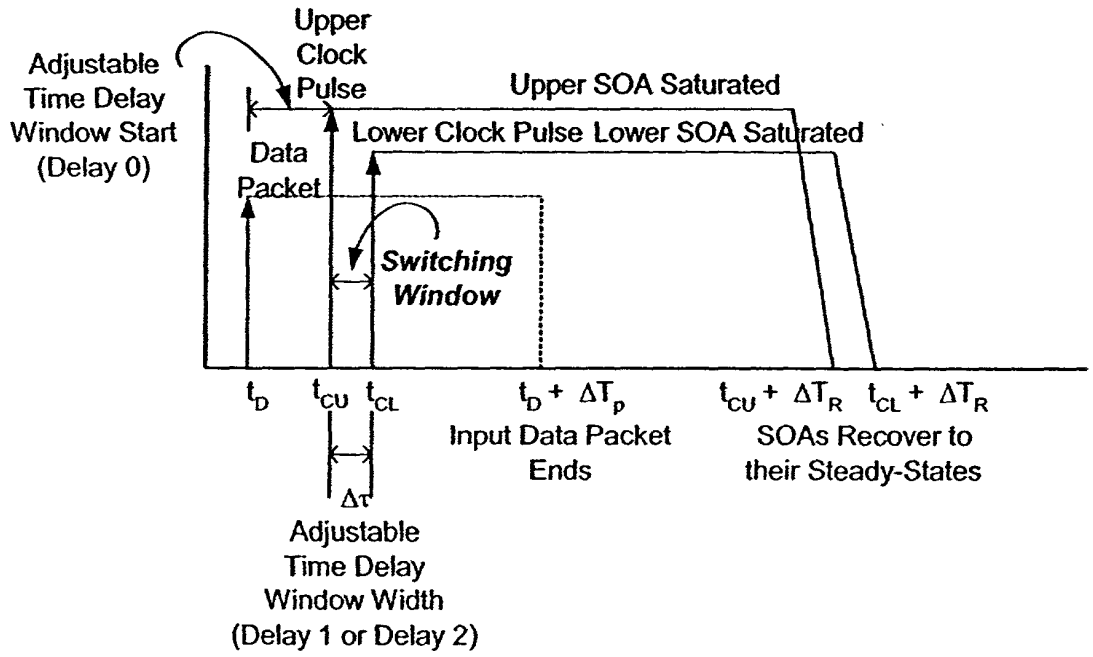
Upper
Clock
Pulse
Adjustable
Time Delay
Window Start
(Delay 0)
Upper SOA Saturated
Lower Clock Pulse Lower SOA Saturated
Data
Packet
Switching
Window
t_D
t_{CU}
t_{CL}
$t_D + \Delta T_p$
$t_{CU} + \Delta T_R$
$t_{CL} + \Delta T_R$
Input Data Packet
Ends
SOAs Recover to
their Steady-States
$\Delta\tau$
Adjustable
Time Delay
Window Width
(Delay 1 or Delay 2)

Fig. 9